## CLAIMS

1. An apparatus for programming an MxN array of reconfigurable processor cells, each cell being operative according to a context instruction, comprising:

an execution mode signal generator, connected to each cell in the array and having an execution mode signal for controlling an execution mode of each cell; and

an enable register connected to the array and providing an enable signal to each cell in the array for controlling delivery of a next context instruction to each enabled cell based on the execution mode.

2. The apparatus of claim 1, wherein the enable register further comprises:

a row enable register connected to each row of the array and having an M-bit row enable signal for controlling an active state of each cell in a row; and

a column enable register connected to each column of the array and having an N-bit column enable signal for controlling an active state of each cell in a column.

3. The apparatus of claim 1, further comprising a context memory, responsive to the enable signal and the execution mode signal, for delivering the next context instruction to each active cell in the array.

4. The apparatus of claim 1, wherein a default state of each cell in the array is an enabled state.

5. The apparatus of claim 1, further comprising an enable signal loader connected to the enable register and responsive to an address signal for selecting a subset of cells in the array for enabling.

6. The apparatus of claim 3, wherein the context memory includes a context register connected to each cell in the array, wherein the context register is connected to the enable signal.

7. A SIMD/MIMD system for processing data, comprising:

an M row x N column array of independently enabled processing cells, wherein each cell includes a context register for storing a context instruction which controls an operation unit of the cell;

an enable register having a row enable register for providing a row enable signal to each row in the array, and a column enable register for providing a column enable signal to each column in the array;

an execution mode generator for generating an execution mode signal for controlling an execution mode of the array; and

a control circuit connected to each processing cell, each control circuit having inputs for receiving the row enable signal, the column enable signal, and the execution mode signal, and including logic that outputs a first control signal for controlling input of the data to the operation unit of the cell, and a second control signal for controlling input of the context instruction to the context register of the cell.

8. The system of claim 7, wherein the execution mode of the array includes:

a SIMD mode in which each enabled cell repeatedly executes on an updated context instruction;

a programming mode in which an plurality of updated contexts are broadcast to the enabled cells, and the function of each cell is not updated; and

a MIMD mode in which the context registers are frozen and each cell executes on its present context; and

9. A method, comprising:

enabling a sub-unit of cells for a new context instruction in an MxN array of cells, wherein each non-enabled cell maintains its present context instruction; and

providing the new context instruction to each cell in the sub-unit.

10. The method of claim 9, wherein each masked cell keeps its internal states and the present context.

11. A method of programming a operations context for a MxN array of cells, comprising:

selecting an execution mode for each cell in the array, wherein the execution mode includes a MIMD execution mode and a SIMD execution mode;

executing, by each cell having the MIMD execution mode, a present context; and

executing, by each cell having the SIMD execution mode, an updated context.

12. A dynamically reconfigurable processing cell for an MxN array of cells , comprising:

a clock signal input for receiving a global clock signal;

at least one functional unit configured to execute an operation;

a context register, connected to each functional unit, configured to output a context instruction that controls each functional unit;

a register file for storing a result from said at least one functional unit;

a first control input connected to the register file for receiving a first enable signal that controls latching of the result from said at least one functional unit by the register file; and

a second control input connected to the context register for receiving a second enable signal that controls latching of a next context instruction by the context register.

13. The cell according to claim 12, wherein the first enable signal is configured to activate the plurality of sequential processing elements.

14. The cell according to claim 12, wherein the second enable signal is configured to activate the context register, wherein the context register is adapted to receive a new context instruction only in the active state.

15. The cell according to claim 12, wherein the first and second inputs are responsive to an enable signal provided by an external enable register.